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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/696,090	10/29/2003	Seung-Jae Chung	5649-1152	6639

7590 10/03/2006

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EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 10/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/696,090	CHUNG ET AL.	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a non-Final Office Action in response to Amendment filed August 25, 2006. Claims 1-24 are presently under examination and still pending.

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d) for the REPUBLIC OF KOREA Application 2002-87246, filed 12/30/2002. The certified copy has been filed in parent Application No. 10/696,090, filed on 10/29/2003.

Response to Arguments

Applicant's arguments, see Remarks filed August 25, 2006, with respect to the rejection of claims 1-24 under 35 U.S.C. 102(e) as being anticipated by Song et al. (US 6,816,990), have been fully considered and are persuasive. Therefore, the rejection has been withdrawn.

However, upon further consideration, a new ground of rejection is made under 35 U.S.C. 102(b) as being anticipated by Pressly et al. (US 5,774,476), as set forth in the present Office Action, below, and therefore Applicant's arguments with respect to claim 1-24 are moot in view of the new ground of rejection, as set forth in the present Office Action, below.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Pressly et al. (US 5,774,476).

Regarding **independent Claims 1, 4, 13, 14, 15, 16, 20, 21**, Pressly discloses an integrated circuit device (10, Figures 1, 2), comprising:

A core block (embedded core 14) having a plurality of inputs and outputs (Abstract) coupled to a speed path test cell (32, Figure 2), which combines most of the functionality of both of the cells 16 and 18 in Figure 1. The core (14) is configured for dynamic simulation testing, such as (speed path testing), wherein core (14) generates core output data at the outputs as illustrated in Figure 2. Also, the circuitry of Figure 1 illustrates a system whereby the embedded core 14 and the customer specified logic 12 can be speed path tested at-speed and simultaneously. Further, in Figure 2, when enabling speed path testing, the multiplexers (38, 40, and 42) can be configured to provide speed path launch capability, through flip-flops 34 and 36, path 1 of multiplexer 38 to an input of the embedded core 14.

An input side sub logic circuit unit (customer specified logic 12) configured for dynamic simulation testing (speed path testing) and coupled to a plurality of input ports (inputs, see Abstract) of the core block 14, which performs most of the communication with the external terminals of the integrated circuit 10 via the inputs and outputs illustrated in Figure 1, and which generates data for the plurality of input ports of the core block 14. According to Pressly, it is important to note, "that both the customer

specified logic 12 and the embedded core 14 will contain a plurality of inputs and a plurality of outputs. Therefore, in most embodiments, a plurality of the cells 16 are resident within the integrated circuit 10, and a plurality of cells 18 are also resident within the integrated circuit 10 to allow for testing of the many inputs and output to the core 14 and the logic 12".

A multiplexer (MUX 42, Figure 2) unit between the core block 14 and the (customer specified logic 12) that selectively provides the (customer specified logic 12) output data (MUX 42 path 0) or the core block 14 output data (MAX 42 path 1) as inputs to the core block 14 in response to a MUX control signal (TRTE1) Figure 2.

The core block 12 generates the core output data for the plurality of output ports, defined as the path coupled to (MUX 40 path 0) and (MAX 42 path 1), in response to the outputs from the (MUX 42).

Regarding Claims 2, 3, 5, Pressly discloses an output side sub logic circuit unit corresponding the input logic part of the customer specified logic 12, which receives data from the outputs of core block 14 via (MUX 40 path 0), as shown in Figure 2.

Regarding Claims 6-12, 17-19, 22-24, Pressly describes a wrapper scan test circuit in reference to Figure 1, which illustrates that the embedded core 14 contains a plurality of internal flip-flops (not specifically illustrated in Figure 1) and which are connected in one or more serial scan chains. Embedded core 14 of Figure 1 illustrates two serial scan chains. Figure 1 illustrates a first scan data input (SDI1), which provides input serial scan data to the first flip-flop in a first plurality of flip-flops, and a first scan data output (SDO1) which provides serially scanned data out from the last flip-flop in a

first plurality of flip-flops within the core 14, to form a first scan chain. A second scan chain of a second plurality of flip-flops within core 14 is formed via a second scan data input (SDI2), which has a second scan data output (SDO2). A wrapper surrounding the embedded core 14 will contain many cells similar to 16 and 18. However, only two cells 16 and 18 are illustrated in Figure 1 by way of example.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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Examiner
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Date: 27 September 2006
Office Action: Non-Final Rejection